

6. The MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor)

Summary of last lecture

1. Band profiles
2. Capacitance
3. I-V characteristics
4. Transconductance

6. The MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor)

Summary of today's lecture

1. Structure and Fabrication
2. Depletion and enhancement mode devices
3. CMOS
4. Moore's Law
5. Scaling

6. The MOSFET

Final thoughts about the I-V characteristic

Recall the I-V characteristic calculated previously. The channel conductance resulted from the inversion charge, and we calculated I_D - V_{DS} .

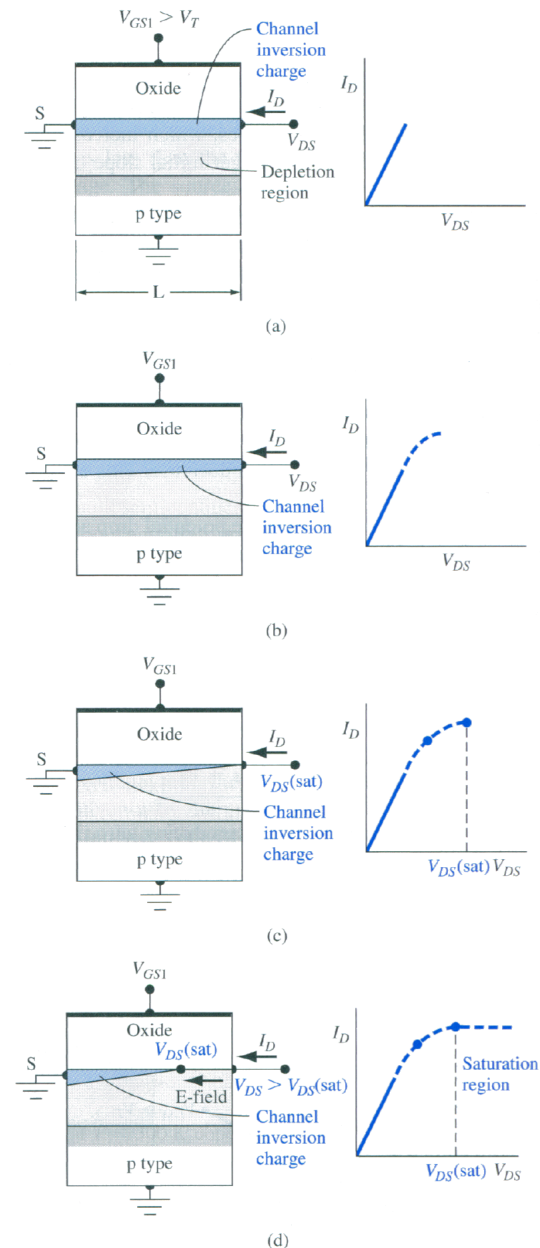
But what happens when $V_{DS} > V_{sat}$?

The point at which the inversion charge is just zero moves towards the source.

Electrons are injected into the space charge region and swept towards the drain. If $\Delta L \ll L$ then I_D will be constant for $V_{DS} > V_{sat}$

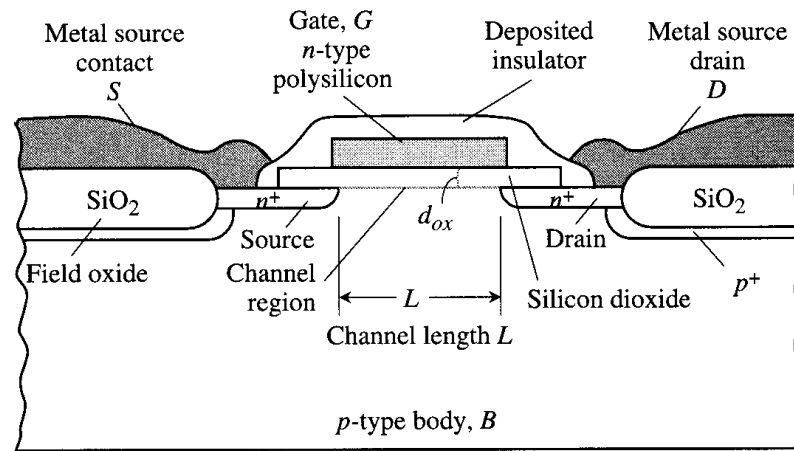
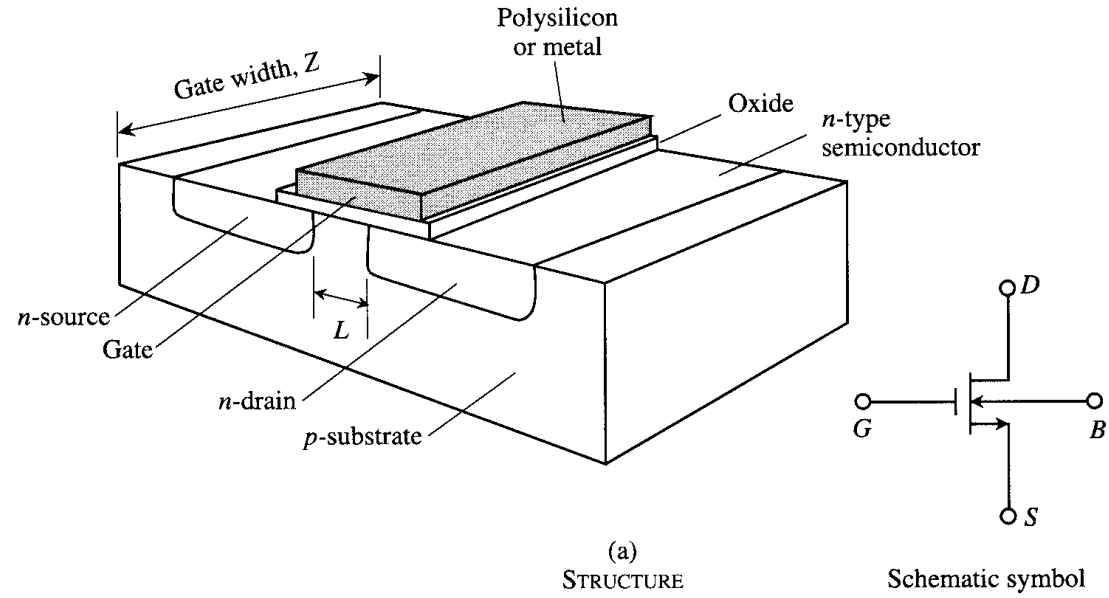
In a MOSFET, unlike a MESFET, charge can be induced *without doping* \rightarrow **no** scattering due to doping and high μ ; **no** carrier freeze-out on dopants.

(However, there are still defect states at the interface and additional scattering by interface roughness).



6. The MOSFET

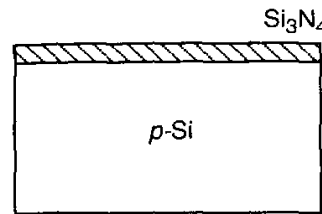
Construction of a MOSFET



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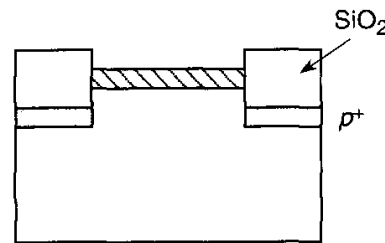
NMOS fabrication

Coat the entire wafer with Si_3N_4 . Si_3N_4 is impervious to dopants.



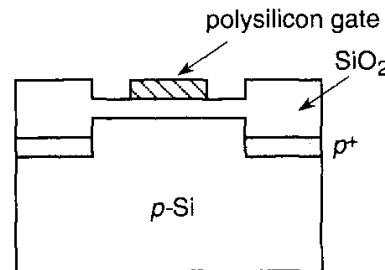
(a)

First mask: Define transistor area and remove Si_3N_4 . Implant p^+ regions to serve as device isolation. Grow thick field oxide.

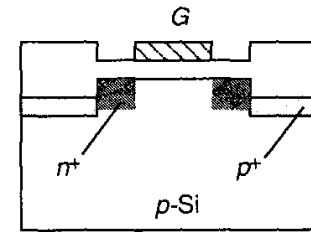


(b)

Etch Si_3N_4 and grow thin gate oxide. On the gate oxide, grow polysilicon and define the gate via a mask.

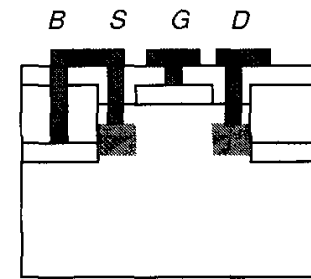


(c)



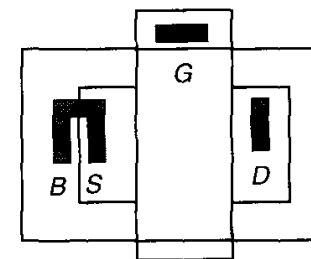
(d)

n^+ source and drain are produced by ion implantation.



(e)

SiO_2 is deposited on the entire structure. A mask is used to open windows for contacts. Al is evaporated.



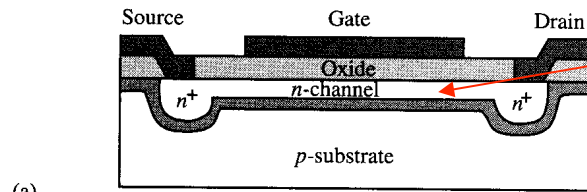
(f)

Top view of the device

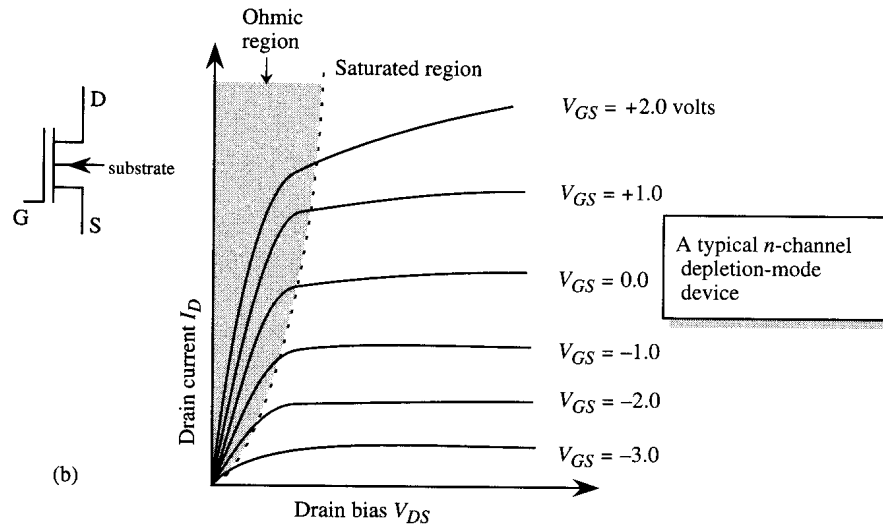
- p^+ implants are done outside the transistor to **isolate the devices** (high-density integration !) by inhibiting formation of an inversion layer under the thicker field oxide
- A **polysilicon** gate is often used to **decrease** V_{th} ;
- Contacts **B-S** (Body-Source) are tied together to ensure there is no **substrate-source** current.
- Since a positive bias is applied to the **drain**, the drain-substrate diode is also switched off.

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The Depletion MOSFET

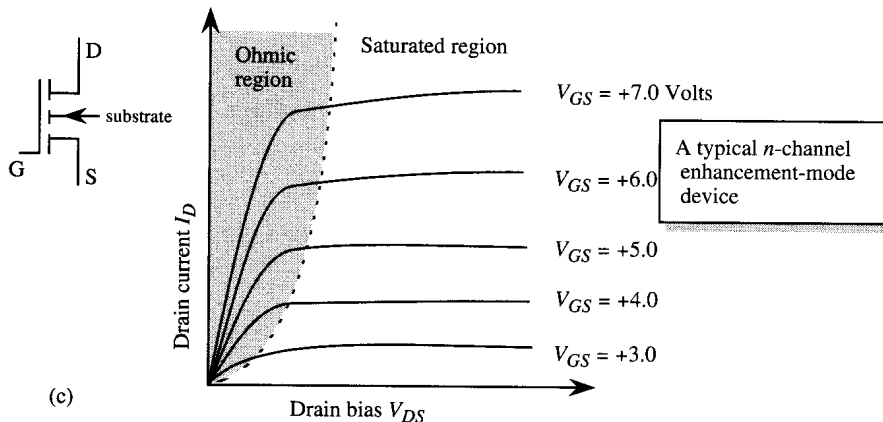


An **additional n^+ layer** is diffused to produce conduction at zero gate voltage.



Current flows at $V_{GS}=0$ and is **switched off** when a gate voltage (*-ive* or *+ive* in general) is applied

Important as a switching device in MOSFET logic.



Enhancement-mode MOSFET (discussed earlier):

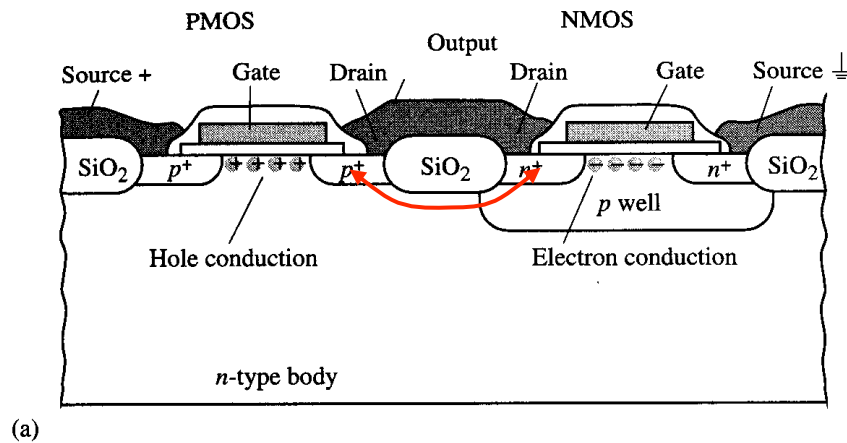
Current does not flow at $V_{GS}=0$ but flows at a gate voltage larger than threshold.

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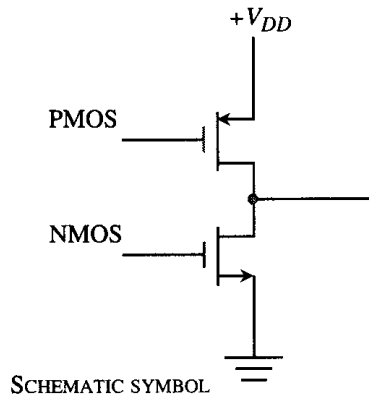
CMOS Technology

Complementary MOSFETs: NMOS and PMOS FETs on one substrate.

Main advantage: low power dissipation.



(a)



(b)

PMOS transistor occupies more chip area than NMOS transistor, to compensate for the lower hole mobility. This allows similar currents in NMOS and PMOS.

“Latch up” has been a major problem for CMOS circuits

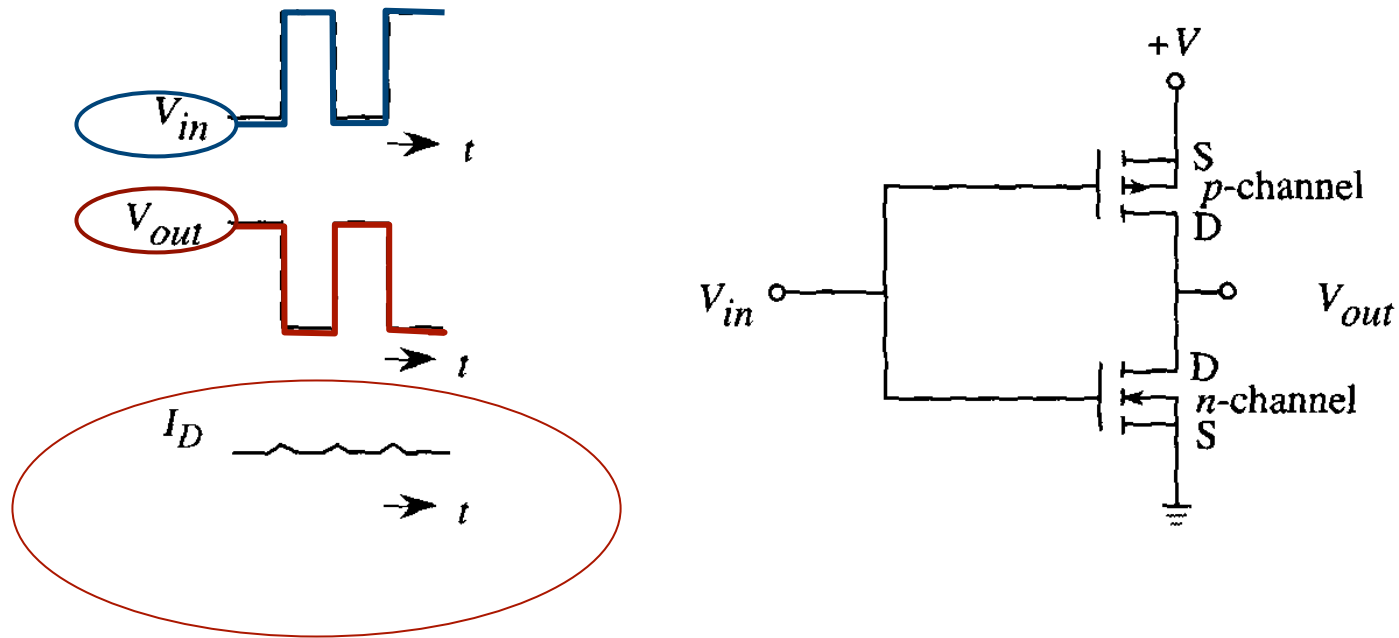
It is a low voltage high current state that may occur in the pnpn structure indicated, and involves the interaction of the parasitic p⁺np and npn⁺ transistors.

Normally both transistors are cut off, but avalanche breakdown in the p well to n substrate region can instead send both into saturation.

Solutions are deep traps to kill the minority carrier lifetime, or insulating regions to isolate the two FETs

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The CMOS FET as an INVERTER



The circuit drives the current ONLY during the input voltage switching !

CMOS is the most popular technology for digital electronics because:

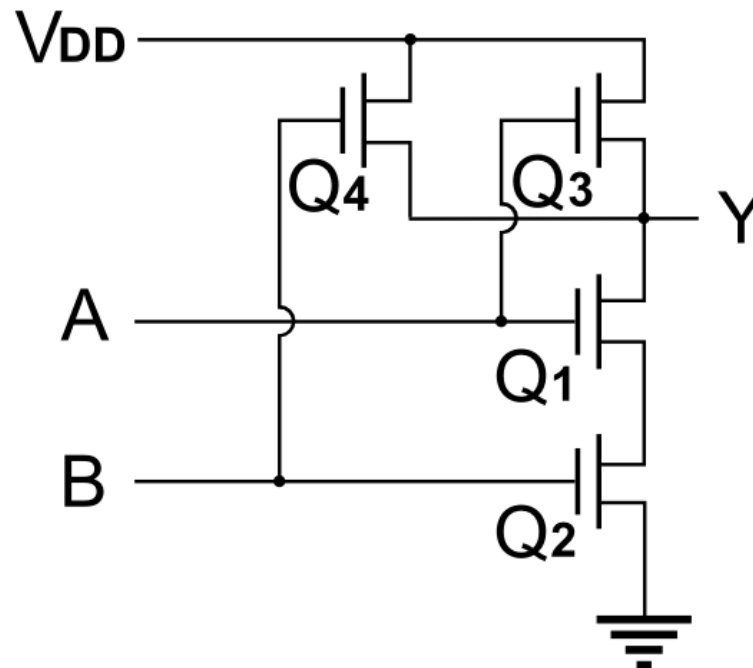
- Of low power dissipation
- The fabrication process lends itself to minaturization

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CMOS based logic

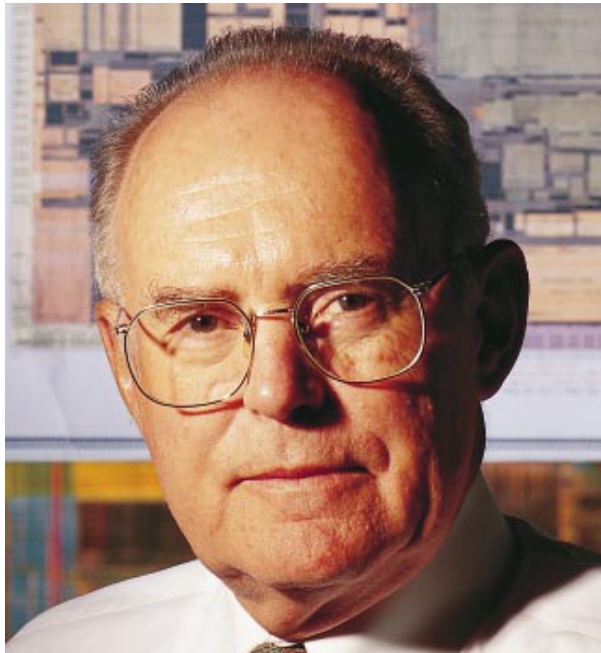
The NAND gate is the basic building block from which all other logic gates can be constructed

CMOS NAND gate



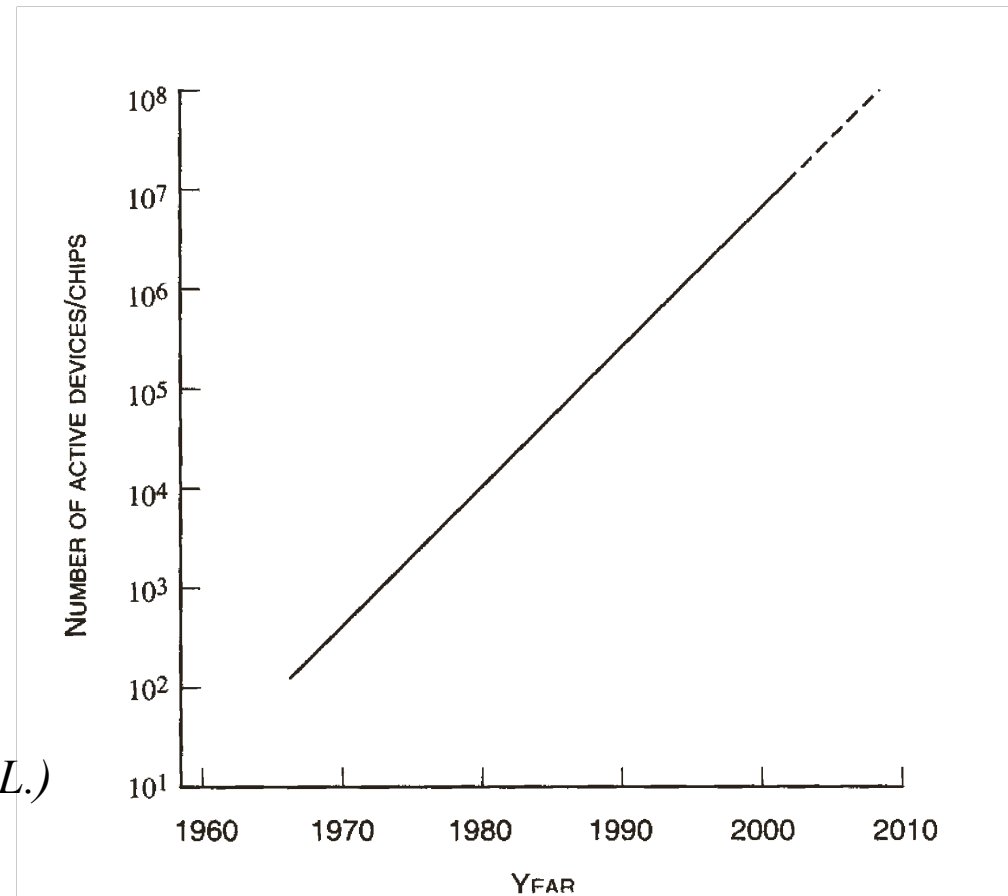
6. The MOSFET

Moore's Law



(Gordon Moore, the co-founder of INTEL.)

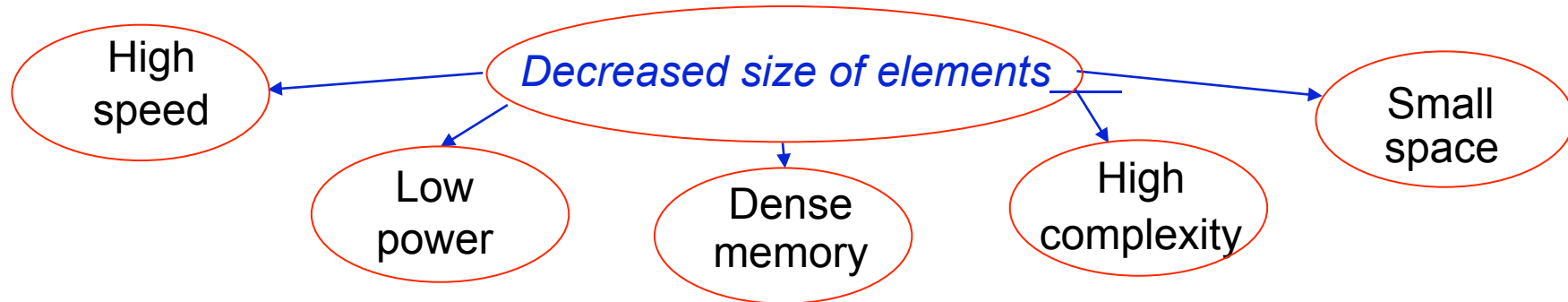
Moore's law: number of active elements on a chip **doubles** every 18 months (59% per year).



Cost reduction of MOS technology:
25-30% per year per function.

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Scaling of MOSFETs in IC technology



Full scaling: All sizes and voltages are decreased by the same factor $K > 1$: so as to maintain same values of electric fields (aka constant field scaling)

$$C_{ox} \propto A/d_{ox} \propto K/K^2 = 1/K \quad C_{ox}^1 (\text{per unit area}) \propto K$$

$$I_D \propto WC_{ox}^1 V^2/L \propto 1/K \times K \times 1/K = 1/K;$$

$$\text{Power} = I_D V_D \propto 1/K \times 1/K = 1/K^2 \quad \text{Switching } t = C_{ox} V_D / I_D \propto 1/K = 1/K.$$

Constant voltage scaling: (to maintain compatibility with previous structures):

$$C_{ox} \propto 1/K \quad C_{ox}^1 (\text{per unit area}) \propto K$$

$$I_D \propto WC_{ox}^1 V^2/L \propto 1/K \times K \times K = K$$

$$\text{Power} = I_D V_D \propto K = K \quad \text{Switching } t = C_{ox} V_D / I_D \propto 1/K \times 1/K \propto 1/K^2$$

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The end of scaling?

Reduction in feature sizes has continued: Intel introduced a 32 nm feature size technology in 2009

BUT clock speeds have not kept pace with increases in device density. Processor architectures are moving to multiple cores rather than high clock speeds. Why?

- CMOS consumes power when switching (due to current need to charge the gate, and also interconnects as the size of the gate decreases) and constant voltage scaling leads to an unacceptable heat load (currently 1 kW/cm² for 45 nm feature size technology)
- There are other dynamic losses: due to the short circuit between the upper supply rail and ground during the transition when the PMOS and NMOS transistor are both on; and due to “glitches”.
- Threshold voltages have been reduced to increase speed and this causes greater passive leakage due to tunneling, and hence power loss. High k dielectrics are intended to avoid this i.e. they provide the same capacitance for thicker gate oxide. However the improvement is not as great as initially appears because high K dielectrics also have a lower barrier height which favours tunneling.
- Sub-threshold leakage occurs due to thermal injection of carriers from the source into the channel even before the inversion layer has formed

Time for a different technology?

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