Quad-phase synchronous light detection with 64 × 64 CMOS modulated light camera

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A scalable 64 × 64 array of feedback buffered photodiodes with column level demodulation circuitry has been fabricated in a 0.35 μm CMOS process. The camera provides two-dimensional phase-sensitive imaging on a line-scan basis using 64 independent quad-phase demodulation channels. Using four phases suppresses even harmonics, enabling the array to be used for heterodyne demodulation.

Introduction: The information of interest in many optical measurements is contained in a small modulated signal on a large constant (DC) background. Such techniques usually employ point measurement with a lock-in amplifier. One example is differential surface plasmon resonance (*d*SPR) imaging [1]. To perform two-dimensional imaging the point measurement system must be used with mechanical scanning, which is slow. The sensor described here has a two-dimensional (2D) array incorporating on-chip demodulation circuitry and is a robust and cost-effective solution for parallel imaging of modulated signals on a large DC background. The camera differs from previous modulated light cameras [2–4] in that it measures AC phase and the (logarithmically compressed) DC level, in contrast to [2], which measures only the AC amplitude, and unlike [3, 4], the quad-phase demodulation scheme allows for the detection of signals hidden within even harmonics of a large magnitude.

Overview of sensor: Each pixel provides a buffered continuous voltage that is logarithmically proportional to the light intensity. Quad-phase detection of the modulated signal is performed in 64 independent column processing channels where each channel consists of a hysteretic differentiating amplifier (HDA) [5] and four switched capacitor demodulators, which provide on-chip averaging as well as demodulation [6]. A 2D image is acquired by integrating one row at a time, and scanning electronically, thus requiring no moving parts. The pixel pitch is 25 μm with a photodiode area of 343 μm^2 providing a fill-factor of 55% and an array size of 1.6 by 1.6 mm on a die of 11 mm^2. Additional circuitry is used to decode the column and row addresses and buffer the analogue outputs. A summary of the technical specifications and a microphotograph of the chip are shown in Table 1 and Fig. 1, respectively.

Table 1: Summary of technical specifications

Pixel pitch (μm)	Output voltage swing (V)	Max pixel rate (channels/s)	Fill factor	Max modulation frequency
25 × 25	2.3 V	>100 kHz (function of modulation frequency and on-chip averaging)	55%	1 MHz

Photodiode array: The outputs of the 64 × 64 pixel photodiode array can be selected on a row-by-row basis and attached to the processing circuitry. Fig. 2 shows the schematic of an individual pixel as used in the array. Each pixel comprises an *n*-well to *p*-substrate photodiode and a transimpedance amplifier with buffered feedback [7]. A voltage controlled current source (Q1) loads the photodiode creating the continuous time behaviour. A high gain amplifier constructed from Q2 and Q3 has its input connected to the cathode of each photodiode and its output fed back to the gate of Q1, which improves the frequency response by reducing the voltage swing at the photodiode cathode and therefore the capacitive charging required of the photocurrent. Q4 enables or disables the amplifier to reduce overall current consumption and Q5 is used to select the pixel output. Q1 is held in weak inversion, hence the gate to source voltage depends logarithmically on the drain current. Pixel bandwidth is thus proportional to the photocurrent, and varies from a few hundred hertz at low light levels to a few megahertz in strong light. The use of a logarithmic pixel is dictated by the requirement of a continuous time signal by the demodulation circuitry and results in a very large dynamic range, but has low contrast. This nonlinear response introduces unwanted harmonics to the modulated signal. While at low modulation depths the total harmonic distortion (THD) is negligible, at larger modulation depths (>25%) it is severe. The greatest contribution to THD [8] is from even harmonics, which are suppressed by the four-channel demodulation technique implemented here.

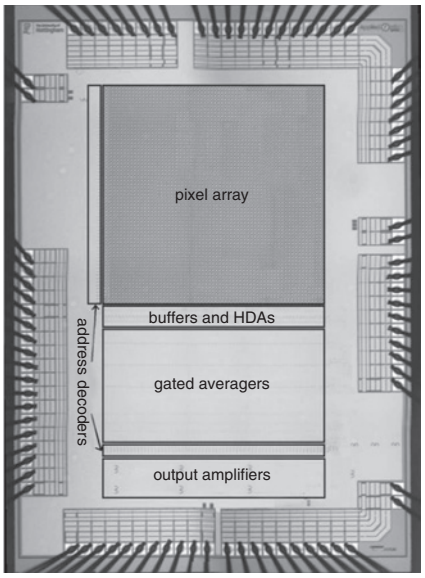

Fig. 1 *Micrograph of camera chip*

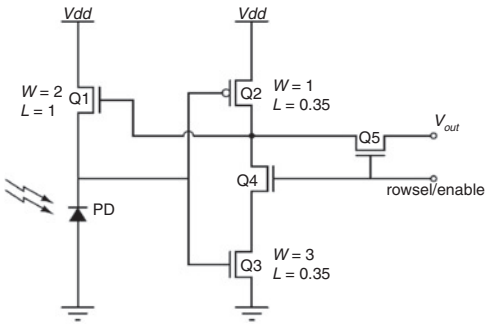

Fig. 2 *Schematic of logarithmic feedback buffered pixel*

Q4 and 5 enable and select the pixel, Q1 behaves as current source controlled by voltage output of high-gain amplifier consisting of Q2 and 3

Synchronous detection circuitry: The synchronous detection circuitry consists of 64 independent quad-phase processing channels (one per column) that share clock and bias lines. Each channel consists of an HDA [5], and a four-phase switched capacitor demodulator. The HDA is an operational transconductance amplifier (OTA) with a lowpass filter (LPF) in the feedback network. It acts as a voltage follower for DC and frequencies below 0.01 Hz (determined by the LPF in the feedback network); however, at higher frequencies the OTA is effectively open-loop and delivers a gain of around 30 dB. A single external resistor sets the bias current for all 64 HDAs and consequently the high frequency cutoff.

Demodulation is performed with a quad-phase switched capacitor demodulator, similar to the dual-channel demodulator introduced by Pitter *et al.* [6, 9]. Fig. 3 shows a schematic of a single switched capacitor demodulator. Each demodulation channel contains four such circuits clocked with non-overlapping clock pairs (phi1 and phi2) at 90° intervals. On the falling edge of phi1 the demodulators sample the amplified signal (at a constant phase) onto a small tunable capacitance consisting of the gate of Q1 plus a selectable combination of Q2–5. This allows for a selectable capacitance ratio (*n*) of 42–6000. When phi2 goes high, the sampled charge is integrated onto the large capacitance Q6. To acquire a measurement a number of sampling and integration cycles are performed resulting in an exponentially weighted temporal average of the input voltage at a particular phase where the ratio of the small (*C*) to the large capacitance (*nC*) determines the degree of averaging. The demodulator can be regarded as a switched capacitor LPF with a time constant of $\tau = f_s n$, where f_s is the switching frequency and n is the

capacitance ratio. After five time constants, the large capacitance is charged to 99% of its final value.

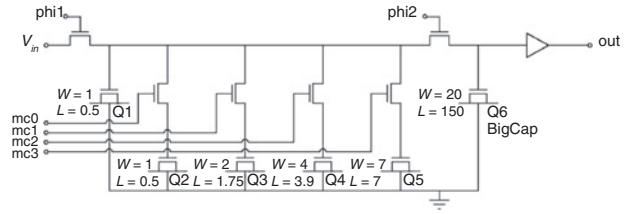

Fig. 3 *Switched capacitor demodulator – circuitry for only single phase shown*

Q1–5 create small capacitance, *C*, with Q1 always being present and Q2–5 being selectable with lines mc0–3. Q6 is big capacitance, *nC*

dSPR imaging with sensor: *d*SPR is extremely sensitive to changes in refractive indices at the boundary of two media [1]. *d*SPR produces an optical signal containing a mixture of the fundamental ($1f$) and ($2f$) of the modulation frequency, where the amplitude of the second harmonic can be much greater than that of the fundamental. As the information of interest is contained within the $1f$ signal, it should be isolated by the camera, and this requires a minimum of four samples per cycle, as presented here. Fig. 4 shows images of protein binding taken with the sensor in a *d*SPR system as described in [1]. A 40 nm-thick gold film is printed with spots of different proteins: human fibrinogen (HFG) and bovine serum albumen (BSA). Anti-BSA is bound to the BSA prior to the beginning of the experiment; the printed proteins that have bound to the anti-BSA are shown as light coloured spots on the left image. Subsequent binding of anti-HFG to the HFG spots causes the additional light regions to appear as the change in refractive index at the gold/analyte interface induces a local change in the plasmon angle; this alters the $1f$ component of the signal measured by the camera.

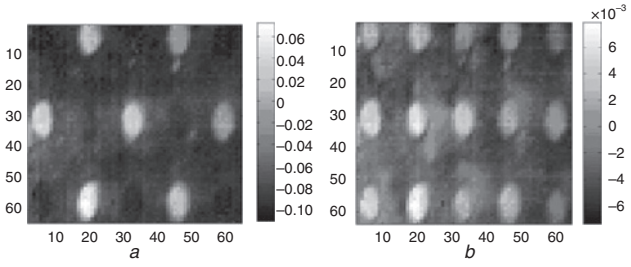

Fig. 4 *Imaging of biological binding with camera*

a BSA and HFG spots printed on sample, anti-BSA has bound to surface of BSA spots increasing magnitude of $1f$ signal making the spots visible, time = 0
b Image of same region after anti-HFG was introduced, time = 20 min after introduction of complementary pattern

Conclusions: A quad-phase synchronous optical sensor with an array of 64 × 64 feedback buffered photodiodes has been fabricated in a 0.35 μm process. Two-dimensional images of the phase, amplitude and DC level of an amplitude modulated optical signal are possible without the need for mechanical scanning. The quad-phase demodulation scheme suppresses even harmonic content of the signal, so the camera is applicable to optical techniques such as *d*SPR imaging where the signal of interest is buried by large even harmonics and measurements where both the fundamental and second harmonic must be measured independently.

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